A CMOS image sensor with a low-power architecture

Abstract of Disclosure

A system of reducing power consumption in and active pixels sensor. The sensor is broken into different blocks, and each of the blocks is individually optimized. The optimization may include minimizing the parasitic capacitance on the readout bus, turning off biases when not in use, and operating in a way that minimizes static power consumption of different elements such as A/D converters.

Figures